IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) A current driver integrated on a semiconductor chip, comprising:

a first current distribution MISFET of a first conductivity type, a source of the first current distribution MISFET being supplied with a supply voltage;

a first current input MISFET of a second conductivity type, a drain of the first current input MISFET being electrically connected to a drain of the first current distribution MISFET, the drain and a gate electrode of the first current input MISFET being electrically connected to each other;

a second current input MISFET of [[a]] the second conductivity type, a gate electrode of the second current input MISFET [[and]] being electrically connected to the gate electrode of the first current input MISFET ~~constituting a current mirror circuit~~, a drain and [[a]] the gate electrode of the second current input MISFET being electrically connected to each other;

~~a first bias line for connecting the gate electrode of the first current input MISFET and the gate electrode of the second current input MISFET;~~

a plurality of current supply sections each including a current source MISFET of the second conductivity type, ~~the current source MISFET, the first current input MISFET and the second current input MISFET constituting a current mirror circuit, a~~ gate ~~electrode~~ electrodes of [[the]] a plurality of current source ~~MISFET~~ MISFETs of the plurality of current supply sections being electrically connected to ~~the first bias line~~ the gate electrodes of the first and second current input MISFETs;

a second current distribution MISFET of the first conductivity type, a gate electrode of the second current distribution MISFET [[and]] being electrically connected to a gate electrode of the first current distribution MISFET ~~constituting a current mirror circuit~~, a drain of the second current distribution MISFET being electrically connected to the drain of the second current input MISFET;

a third current distribution MISFET of the first conductivity type provided adjacent to the second current distribution MISFET, a gate electrode of the third current distribution MISFET[[,]] being electrically connected to the gate electrodes of the first current distribution MISFET and the second current distribution MISFET ~~constituting a current mirror circuit~~; and

a first current output terminal ~~which is~~ being electrically connected to a drain of the third current distribution MISFET.

2. (Currently Amended) The current driver of claim 1, wherein [[the]] a distance between the second current distribution MISFET and the third current distribution MISFET is equal to or shorter than 200 um.

3. (Currently Amended) The current driver of claim 1, further comprising a bias power supplying terminal ~~which is~~ being electrically connected to the gate electrode of the second current distribution MISFET and the gate electrode of the third current distribution MISFET.

4. (Currently Amended) The current driver of claim 1, further comprising:

~~at least one~~ an additional current distribution MISFET of the first conductivity type provided in a region of the semiconductor chip which is distant from the third current distribution MISFET by 200 um or less, a gate electrode of the additional current distribution MISFET[[,]] being electrically connected to the gate electrodes of the second current distribution MISFET and the third current distribution MISFET ~~constituting a current mirror~~; and

an additional current output terminal ~~which is~~ being electrically connected to ~~each of the at least one~~ a drain of the additional current distribution MISFET.

5. (Currently Amended) The current driver of claim 1, further comprising:

a first cascode MISFET of the first conductivity type which is provided between the first current distribution MISFET and the first current input MISFET;

a second cascode MISFET of the first conductivity type which is provided between the second current distribution MISFET and the second current input MISFET;

a third cascode MISFET of the first conductivity type which is provided between the third current distribution MISFET and the first current output terminal; and

a first gate bias line ~~which is commonly~~ being electrically connected to [[the]] gate electrodes of the first cascode MISFET, the second cascode MISFET and the third cascode MISFET, one end of the first gate bias line being electrically connected to [[the]] a node supplying a first constant-voltage power supply.

6. (Currently Amended) The current driver of claim 1, further comprising:

a fourth cascode MISFET of the second conductivity type which is provided between the first current distribution MISFET and the first current input MISFET, [[the]] a drain of the fourth cascode MISFET being electrically connected to the gate electrode of the first current input MISFET;

a fifth cascode MISFET of the second conductivity type which is provided between the second current distribution MISFET and the second current input MISFET, [[the]] a drain of the fifth cascode MISFET being electrically connected to the gate electrode of the second current input MISFET;

a plurality of sixth cascode ~~MISFET~~ MISFETs of the second conductivity type, ~~which is~~ each of the plurality of sixth cascode MISFETs being electrically connected to ~~drains~~ each drain of each of the plurality of current source MISFETs of the plurality of current supply sections; and

a second gate bias line ~~which is commonly~~ being electrically connected to [[the]] gate ~~electrode~~ electrodes of the fourth cascode MISFET, ~~the gate electrode of~~ the fifth cascode MISFET and ~~the gate electrode of~~ the plurality of sixth cascode ~~MISFET~~ MISFETs, one end of the second gate bias line being electrically connected to a node supplying a second constant-voltage power supply.

7-8. (Canceled)

9. (Currently Amended) ~~The current driver of claim 8, further comprising:~~ A current driver integrated on a semiconductor chip, comprising:

a first current input terminal;

a first current input MISFET of a first conductivity type, a drain of the first current input MISFET being electrically connected to the first current input terminal, and the drain and a gate electrode of the first current input MISFET being electrically connected to each other;

a plurality of current supply sections each including a current source MISFET of the first conductivity type, each gate electrode of a plurality of current source MISFETs of the plurality of current supply sections being electrically connected to the gate electrode of the first current input MISFET;

a second current input MISFET of the first conductivity type, a drain and a gate electrode of the second current input MISFET being electrically connected to each other, the gate electrode of the second current input MISFET [[and]] being electrically connected to the gate electrode of

the first current input MISFET ~~constituting a current mirror circuit between which the plurality of current supply sections are provided~~;

a bias power input terminal;

a first current distribution MISFET of [[the]] a second conductivity type, a gate electrode of the first current distribution MISFET being electrically connected to the bias power input terminal, [[the]] a drain of the first current distribution MISFET being electrically connected to the drain of the second current input MISFET;

a second current distribution MISFET of the second conductivity type provided in a region of the semiconductor chip which is distant from the first current distribution MISFET by 200 um or less, a gate electrode of the second current distribution MISFET [[and]] being electrically connected to the gate electrode of the first current distribution MISFET ~~constituting a current mirror~~;

a first current output terminal ~~which is~~ being electrically connected to [[the]] a drain of the second current distribution MISFET; and

a first bias power output terminal ~~which is~~ being electrically connected to the gate electrode of the second current distribution MISFET.

10. (Currently Amended) ~~The current driver of claim 8, further comprising:~~ A current driver integrated on a semiconductor chip, comprising:

a first current input terminal;

a first current input MISFET of a first conductivity type, a drain of the first current input MISFET being electrically connected to the first current input terminal, and the drain and a gate electrode of the first current input MISFET being electrically connected to each other;

a plurality of current supply sections each including a current source MISFET of the first conductivity type, each gate electrode of a plurality of current source MISFETs of the plurality of current supply sections being electrically connected to the gate electrode of the first current input MISFET;

a [[third]] second current input MISFET of the first conductivity type, a drain and a gate electrode of the [[third]] second current input MISFET being electrically connected to each other, the gate electrode of the [[third]] second current input MISFET [[and]] being electrically connected to the gate electrode of the first current input MISFET ~~constituting a current mirror circuit between which the plurality of current supply sections are provided~~; and

a second current input terminal ~~which is~~ being electrically connected to the drain of the [[third]] second current input MISFET.

11. (Canceled)

12. (Currently Amended) ~~The current driver of claim 8, further comprising:~~ A current driver integrated on a semiconductor chip, comprising:

a first current input terminal;

a first current input MISFET of a first conductivity type, a drain of the first current input MISFET being electrically connected to the first current input terminal, and the drain and a gate electrode of the first current input MISFET being electrically connected to each other;

a plurality of current supply sections each including a current source MISFET of the first conductivity type, each gate electrode of a plurality of current source MISFETs of the plurality of current supply sections being electrically connected to the gate electrode of the first current input MISFET;

a current output MISFET of the first conductivity type, a gate electrode of the current output MISFET being electrically connected ~~between~~ to the gate electrode of the first current input MISFET and the gate electrodes of the plurality of current source MISFETs;

~~a current-voltage converter which is connected to a drain of the current output MISFET;~~

a first current distribution MISFET of a second conductivity type, a drain and a gate electrode of the first current distribution MISFET being electrically connected to each other, the drain of the first current distribution MISFET being electrically connected to a drain of the current output MISFET;

a ~~fourth~~ second current input MISFET of the first conductivity type, a drain and a gate electrode of the ~~fourth~~ second current input MISFET being electrically connected to each other, ~~fourth~~ the gate electrode of the second current input MISFET [[and]] being electrically connected to the gate electrode of the first current input MISFET ~~constituting a current mirror circuit between which the plurality of current supply sections are provided~~;

a [[third]] second current distribution MISFET of the second conductivity, ~~having~~ a gate electrode of the second current distribution MISFET being electrically connected to ~~the current-voltage converter~~ the gate electrode of the first current distribution MISFET and a drain of the second current distribution MISFET being electrically connected to the drain of the ~~fourth~~ second current input MISFET;

a ~~fourth~~ third current distribution MISFET of the second conductivity provided in a region of the semiconductor chip which is distant from the [[third]] second current distribution MISFET by 200 um or less, a gate electrode of the ~~fourth~~ third current distribution MISFET [[and]] being electrically connected to the gate electrode of the [[third]] second current distribution MISFET ~~constituting a current mirror~~; and

a ~~second~~ first current output terminal ~~which is~~ being electrically connected to a drain of the ~~fourth~~ third current distribution MISFET.

13-24. (Canceled)

25. (New) A current driver integrated on a semiconductor chip, comprising:

a first current distribution MISFET of a first conductivity type;

a first current input MISFET of a second conductivity type, a drain of the first current input MISFET being electrically connected to a drain of the first current distribution MISFET, the drain and a gate electrode of the first current input MISFET being electrically connected to each other;

a second current input MISFET of the second conductivity type, a gate electrode of the second current input MISFET being electrically connected to the gate electrode of the first current input MISFET, a drain and the gate electrode of the second current input MISFET being electrically connected to each other;

a plurality of current supply sections each including a current source MISFET of the second conductivity type, a plurality of current source MISFETs of the plurality of current supply sections being between the first current input MISFET and second current input MISFET and gate electrodes of the plurality of current source MISFETs being electrically connected to the gate electrodes of the first and second current input MISFETs;

a second current distribution MISFET of the first conductivity type, a gate electrode of the second current distribution MISFET being electrically connected to a gate electrode of the first current distribution MISFET, a drain of the second current distribution MISFET being electrically connected to the drain of the second current input MISFET;

a third current distribution MISFET of the first conductivity type, a gate electrode of the third current distribution MISFET being electrically connected to the gate electrodes of the first current distribution MISFET and the second current distribution MISFET; and

a first current output terminal being electrically connected to a drain of the third current distribution MISFET.

26. (New) The current driver of claim 25, wherein the plurality of current source MISFETs of the plurality of current supply sections are formed in a region between the first current input MISFET and second current input MISFET.

27. (New) The current driver of claim 25, wherein the plurality of current source MISFETs of the plurality of current supply sections are formed in a region extending between the first current input MISFET and second current input MISFET.

28. (New) The current driver of claim 25, wherein a distance between the second current distribution MISFET and the third current distribution MISFET is equal to or shorter than 200 um.

29. (New) The current driver of claim 25, further comprising:

a bias power supplying terminal being electrically connected to the gate electrode of the second current distribution MISFET and the gate electrode of the third current distribution MISFET.

30. (New) The current driver of claim 25, further comprising:

an additional current distribution MISFET of the first conductivity type, a gate electrode of the additional current distribution MISFET being electrically connected to the gate electrodes of the second current distribution MISFET and the third current distribution MISFET; and

an additional current output terminal being electrically connected to a drain of the additional current distribution MISFET.

31. (New) The current driver of claim 25, further comprising:

a first cascode MISFET of the first conductivity type being provided between the first current distribution MISFET and the first current input MISFET;

a second cascode MISFET of the first conductivity type being provided between the second current distribution MISFET and the second current input MISFET;

a third cascode MISFET of the first conductivity type being provided between the third current distribution MISFET and the first current output terminal,

wherein gate electrodes of the first cascode MISFET, the second cascode MISFET and the third cascode MISFET are electrically connected to a node supplying a first constant-voltage power supply.

32. (New) The current driver of claim 25, further comprising:

a fourth cascode MISFET of the second conductivity type being provided between the first current distribution MISFET and the first current input MISFET, a drain of the fourth cascode MISFET being electrically connected to the gate electrode of the first current input MISFET;

a fifth cascode MISFET of the second conductivity type being provided between the second current distribution MISFET and the second current input MISFET, a drain of the fifth cascode MISFET being electrically connected to the gate electrode of the second current input MISFET;

a plurality of sixth cascode MISFETs of the second conductivity type, each of the plurality of sixth cascode MISFETs being electrically connected to each drain of the plurality of current source MISFETs,

wherein gate electrodes of the fourth cascode MISFET, the fifth cascode MISFET and the plurality of sixth cascode MISFETs are electrically connected a node supplying to a second constant-voltage power supply.

33. (New) A current driver integrated on a semiconductor chip, comprising:

a first current input terminal;

a first current input MISFET of a first conductivity type, a drain of the first current input MISFET being electrically connected to the first current input terminal, and the drain and a gate electrode of the first current input MISFET being electrically connected to each other;

a second current input MISFET of the first conductivity type, a drain and a gate electrode of the second current input MISFET being electrically connected to each other, the gate electrode of the second current input MISFET being electrically connected to the gate electrode of the first current input MISFET;

a plurality of current supply sections each including a current source MISFET of the first conductivity type, a plurality of current source MISFETs of the plurality of current supply sections being between the first current input MISFET and the second current input MISFET and each gate electrode of the plurality of current source MISFETs being electrically connected to the gate electrodes of the first and second current input MISFETs;

a bias power input terminal;

a first current distribution MISFET of a second conductivity type, a gate electrode of the first current distribution MISFET being electrically connected to the bias power input terminal, a

drain of the first current distribution MISFET being electrically connected to the drain of the second current input MISFET;

a second current distribution MISFET of the second conductivity type, a gate electrode of the second current distribution MISFET being electrically connected to the gate electrode of the first current distribution MISFET;

a first current output terminal being electrically connected to a drain of the second current distribution MISFET; and

a first bias power output terminal being electrically connected to the gate electrode of the second current distribution MISFET.

34. (New) The current driver of claim 33, wherein the plurality of current source MISFETs of the plurality of current supply sections are formed in a region between the first current input MISFET and second current input MISFET.

35. (New) The current driver of claim 33, wherein the plurality of current source MISFETs of the plurality of current supply sections are formed in a region extending between the first current input MISFET and second current input MISFET.

36. (New) A current driver integrated on a semiconductor chip, comprising:

a first current input terminal;

a first current input MISFET of a first conductivity type, a drain of the first current input MISFET being electrically connected to the first current input terminal, and the drain and a gate electrode of the first current input MISFET being electrically connected to each other;

a second current input MISFET of the first conductivity type, a drain and a gate electrode of the second current input MISFET being electrically connected to each other, the gate electrode

of the second current input MISFET being electrically connected to the gate electrode of the first current input MISFET;

a plurality of current supply sections each including a current source MISFET of the first conductivity type, a plurality of current source MISFETs of the plurality of current supply sections being between the first current input MISFET and the second current input MISFET and each gate electrode of the plurality of current source MISFETs being electrically connected to the gate electrodes of the first and second current input MISFETs; and

a second current input terminal being electrically connected to the drain of the second current input MISFET.

37. (New) The current driver of claim 36, wherein the plurality of current source MISFETs of the plurality of current supply sections are formed in a region between the first current input MISFET and second current input MISFET.

38. (New) The current driver of claim 36, wherein the plurality of current source MISFETs of the plurality of current supply sections are formed in a region extending between the first current input MISFET and second current input MISFET.

39. (New) A current driver integrated on a semiconductor chip, comprising:

a first current input terminal;

a first current input MISFET of a first conductivity type, a drain of the first current input MISFET being electrically connected to the first current input terminal, and the drain and a gate electrode of the first current input MISFET being electrically connected to each other;

a second current input MISFET of the first conductivity type, a drain and a gate electrode of the second current input MISFET being electrically connected to each other, the gate

electrode of the second current input MISFET being electrically connected to the gate electrode of the first current input MISFET;

a plurality of current supply sections each including a current source MISFET of the first conductivity type, a plurality of current source MISFETs of the plurality of current supply sections being between the first current input MISFET and the second current input MISFET and each gate electrode of the plurality of current source MISFETs being electrically connected to the gate electrodes of the first and second current input MISFETs;

a current output MISFET of the first conductivity type, a gate electrode of the current output MISFET being electrically connected to the gate electrodes of the first and second current input MISFETs and the gate electrodes of the plurality of current source MISFETs;

a first current distribution MISFET of a second conductivity type, a drain and a gate electrode of the first current distribution MISFET being electrically connected to each other, the drain of the first current distribution MISFET being electrically connected to a drain of the current output MISFET;

a second current distribution MISFET of the second conductivity type, a gate electrode of the second current distribution MISFET being electrically connected to the gate electrode of the first current distribution MISFET and a drain of the second current distribution MISFET being electrically connected to the drain of the second current input MISFET;

a third current distribution MISFET of the second conductivity type, a gate electrode of the third current distribution MISFET being electrically connected to the gate electrodes of the first and second current distribution MISFETs; and

a first current output terminal being electrically connected to a drain of the third current distribution MISFET.

40. (New) The current driver of claim 39, wherein the plurality of current source MISFETs of the plurality of current supply sections are formed in a region between the first current input MISFET and second current input MISFET.

41. (New) The current driver of claim 39, wherein the plurality of current source MISFETs of the plurality of current supply sections are formed in a region extending between the first current input MISFET and second current input MISFET.